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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
MIKHAYLICHENKO et al.	Docket No. LAM2P316
Application No. 10/033,644	Group Art Unit: 2823
Filed: December 27, 2001	Examiner: Nguyen, Khiem D.
For: METHOD FOR POST-ETCH AND STRIP RESIDUE REMOVAL ON CORAL FILMS	Date: February 8, 2005

CERTIFICATE OF MAILING

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Signed: _____
Edmund H. Mizumoto

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION -- 37 CFR 41.67)

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is in furtherance of the Notice of Appeal received by the United States Patent and Trademark Office on November 8, 2004. This Appeal Brief is transmitted in duplicate.

This application is on behalf of:

☐ Small Entity ☒ Large Entity

Pursuant to 37 CFR 41.20(b)(2), the fee for filing the Appeal Brief is:

☐ $250.00 (Small Entity) ☒ $500.00 (Large Entity)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

02/15/2005 AWONDAF1 00000052 10033644
02 FC:1251 120.00 OP

☒ Applicants petition for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Months	Large Entity	Small Entity
☒ one	$ 120.00	$ 60.00
☐ two	$ 450.00	$225.00
☐ three	$1,020.00	$510.00
☐ four	$1,590.00	$795.00

If an additional extension of time is required, please consider this a petition therefor.

☐ An extension for __ months has already been secured and the fee paid therefor of $ is deducted from the total fee due for the total months of extension now requested.

☐ Applicants believe that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Total Fees Due:

Appeal Brief Fee	$500.00
Extension Fee (if any)	$120.00
Total Fee Due	**$620.00**

☒ Enclosed is Check No. 13482 in the amount of $620.00.

☒ The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-0850 (Order No. LAM2P316). Two copies of this transmittal are enclosed.

Respectfully submitted,
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE Mikhaylichenko et al.

Application for Patent

Filed December 27, 2001

Application No. 10/033,644

FOR:

METHOD FOR POST-ETCH AND STRIP RESIDUE REMOVAL ON CORAL FILMS

APPEAL BRIEF

CERTIFICATE OF MAILING

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APPENDIX A - CLAIMS ON APPEAL

I. REAL PARTY IN INTEREST

The real party in interest is Lam Research Corporation, the assignee of the present invention.

II. RELATED APPEALS AND INTERFERENCES

The undersigned is not aware of any related appeals and/or interferences.

III. STATUS OF THE CLAIMS

Claims 1-24 are pending in the subject application, have been finally rejected, and are on appeal.

IV. STATUS OF AMENDMENTS

Applicants have not submitted any amendment subsequent to final rejection of August 4, 2004.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The subject invention is generally directed toward a cleaning solution for cleaning semiconductor wafers after plasma etch operations. In one embodiment, the invention is directed to a method of removal of residues on a wafer after the etching of materials having low dielectric constant (low-K material), removal of photoresist through ashing, and the subsequent in-situ removal of etching and photoresist residues in the etch chamber.

Independent claim 1 provides a method for cleaning a semiconductor wafer which includes plasma etching a feature into a low K dielectric layer having a photoresist mask where the plasma etching generates etch residues. The method further includes ashing the semiconductor wafer to remove the photoresist mask where the ashing generates ashing residues. The method further includes removing the etching residues and the ashing residues from the low K dielectric layer having the plasma etched feature. The removing

is enhanced by scrubbing the low K dielectric layer of the semiconductor wafer with a wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent.

Independent claim 9 defines a method for cleaning a semiconductor wafer which includes plasma etching a feature into a low K dielectric layer where the plasma etching generates etch residues in and around the feature. The method also includes subjecting the semiconductor wafer to an ashing operation where the ashing operation generates ashing residues. The method further includes scrubbing the low K dielectric layer having the plasma etched feature and using a mixture fluid including a cleaning chemistry and a wetting agent where the wetting agent conditions the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry.

Independent claim 17 provides a method for cleaning a semiconductor wafer which includes plasma etching a feature into a low K dielectric layer where the plasma etching generates etch residues in and around the feature. The method also includes subjecting the semiconductor wafer to an ashing operation where the ashing operation generates ashing residues. The method further includes scrubbing the low K dielectric layer having the plasma etched feature and using a mixture fluid including a cleaning chemistry and a wetting agent where the wetting agent conditions the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry. The method additionally includes scrubbing the low K dielectric layer having the plasma etched feature and using the brush while applying deionized (DI) water after removing the etching residues and the ashing residues.

In general, the claimed invention effectively cleans semiconductor substrates by removing residues from the processes of etching low-K materials and ashing photoresist. Figures 2A through 3C of the specification show exemplary cleaning units and their respective orientation in which substrates that utililize low K dielectrics can be processed

and cleaned. The flowcharts of Figures 4 and 5 describe exemplary method operations that can be performed to clean wafers with low K dielectric features after etching and ashing operations.

Figure 4 shows a flowchart where operation 202 provides a photoresist patterned low K dielectric layer of a semiconductor wafer where the low K dielectric layer is hydrophobic. (see e.g., Specification, page 14 lines 3-10) Then operation 204 performs a plasma etch operation to etch the low K dielectric layer where the plasma etch generates etch residues. (See e.g., Specification, page 14, lines 11-18) After operation 204, the method moves to operation 206 where an ashing operation is performed to remove the photoresist where the ashing operation leaves some ashing residues. (See e.g., Specification, page 14, lines 21-24) Then operation 208 performs a brush scrubbing operation using a fluid mixture including a cleaning chemistry and a wetting agent to remove residues from the low K dielectric layer. (See e.g., Specification, page 15, line 1 to page 18 line 3)

Because low-K materials are hydrophobic, the claimed invention utilizes a wetting agent with a cleaning solution to effectively clean etching and ashing residues from the surface of the newly defined features on the wafer surface. Ashing the photoresist in the etch chamber provides a method of removing polymer and other organic materials from the wafer surface, feature sidewalls and the reactor, changing the composition of remaining materials. Because of the removal of polymers and organic materials by the O_2 plasma ashing process, the silicon content and residual metals are more concentrated and hardened. The claimed invention provides for scrubbing the surface of the wafer with a wetting agent and cleaning chemistry tailored for the low-K material and the byproducts from the etching and ashing operations.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 8, 9, 10, and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of Apelgren et. al. (U.S. Patent No. 6,315,637) ("Apelgren").

Claims 2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Apelgren and further in view of Yoon et. al. (U.S. Publication 2002/0090784) ("Yoon").

VII. ARGUMENTS

Applicants respectfully submit that the Examiner did not properly apply 35 U.S.C. § 103(a) in formulating the Final Rejection of August 4, 2004. Specifically, in accordance with the MPEP §2141 and *Hodosh v. Block Drug Co., Inc.,* 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986), the claimed invention must be considered as a whole, the references must be considered as a whole and must suggest the desirability and thus obviousness of making the combination, the references must be viewed without benefit of impermissible hindsight vision afforded by the claimed invention, and there must be a reasonable expectation of success.

The basic elements required to prove a *prima facie* case of obviousness as set forth in MPEP 2143 are not met by the references when both the invention and references are considered as a whole, and without benefit of impermissible hindsight. Specifically, the

prior art fails to teach each and every limitation set forth in the claims and there was no suggestion or motivation to combine the references.

A. The Examiner Has Failed to Satisfy a Prima Facie Case of Obviousness as the Cited Prior Art References Fail to Provide or Suggest All Claim Features of Claims 1, 8, 9, 10, and 17.

Claims 1, 8, 9, 10, and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of Apelgren et al. ("Apelgren"). This rejection is traversed. Applicants submit that the AAPA and Apelgren do not disclose or suggest all of the features of the claimed invention, and therefore, the Examiner has failed to provide a prima facie case of obviousness against claims 1, 8, 9, 10, and 17.

Independent claim 1 includes the feature of removing the etching residues and the ashing residues from the low K dielectric layer having the plasma etched feature where the removing is enhanced by scrubbing the low K dielectric layer of the semiconductor wafer with a wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent. Independent claim 9 includes the feature of scrubbing the low K dielectric layer having the plasma etched feature and using a mixture fluid including a cleaning chemistry and a wetting agent where the wetting agent conditions the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry. Independent claim 17 includes the feature of scrubbing the low K dielectric layer having the plasma etched feature and using a mixture fluid including a cleaning chemistry and a wetting agent where the wetting agent conditions the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry.

Therefore, claims 1, 9, and 17 include the feature of scrubbing the low K dielectric layer having the plasma etched feature using a mixture fluid including a cleaning

chemistry and a wetting agent to remove/clean etch residues and the ashing residues from the low K dielectric layer. Applicants submit that Apelgren and the AAPA, individually or in combination do not disclose or suggest this claimed feature.

Apelgren is directed towards a method of removing photoresist through chemical mechanical polishing (CMP) and cleaning the remnants of the photoresist layer after the CMP operation. Apelgren provides a method of cleaning remaining post-etch photoresist after the CMP operation by exposing the wafer to dilute HF or de-ionized water (See Apelgren, col. 5 lines 23-29). As known to those skilled in the art, a CMP process of removing resist generally leaves behind a very different material compared to the dry ashing process because the CMP process is wet. Any chemical additives in the polishing slurry will likely soften the photoresist and make it easier to remove. As further known to those skilled in the art, such additives could adjust the pH to aid in hydrolyzing the residues, add an oxidizing species, or undercut the photoresist with a mild etchant. Therefore, the photoresist may be hydrolyzed, swollen, undercut, and rendered hydrophilic by these CMP chemicals. All of these chemical additions would make post-etch residue easier to remove by the subsequent clean. As can be seen in column 5, lines 23-30 Apelgren clearly only teaches the use of a post-CMP scrub with HF, water, or megasonics to remove the remants of the layer of photoresist but does not disclose, suggest, or even mention the possibility of using a wetting agent such as a surfactant that can render a hydrophobic substance cleanable by the cleaning chemistry.

In contrast, as known to those skilled in the art, the ashing process primarily removes the photoresist and does little to remove the post-etch residues and in fact may harden those residues due to more cross-linking of the chemical bonds, better adhesion to the substrate, and a more hydrophobic surface. The burden of removing the post-etch residues therefore lies with the subsequent clean rather than the ashing process.

Consequently, Applicants submit that the cleaning of etching and ashing residues as claimed is not the same as cleaning of a substrate after a CMP operation. As a result, Applicants submit that the feature of scrubbing the low K dielectric layer having the plasma etched feature using a mixture fluid including a cleaning chemistry and a wetting agent to remove/clean etch residues and the ashing residues from the low K dielectric layer is not disclosed or suggested by Apelgren.

Applicants' background (AAPA pages 1-3) discloses that traditional methods of cleaning oxide films are inadequate for the cleaning of hydrophobic low-K dielectrics because typical oxides are hydrophilic and form different types of residues which require different types of cleaning methodology as compared to low K dielectrics (See, Specification, page 3, lines 13-17). In addition, in contrast to Apelgren which discusses cleaning post CMP, the AAPA discusses difficulties in cleaning of residues of etching and ashing operations from low K dielectrics. Applicants note that AAPA does not disclose, suggest, or even mention usage of wetting agents. Therefore, Apelgren and AAPA, individually or in combination do not discuss or suggest using a wetting agent with a cleaning solution to clean etching and ashing residues on a hydrophobic material such as low-K dielectrics.

Consequently, Apelgren and AAPA individually or in combination do not disclose or suggest all of the features of claims 1, 8, 9, 10, and 17. As a result, Applicants submit that the Examiner has failed to provide a prima facie case of obviousness against claims 1, 8, 9, 10, and 17.

B. The Examiner Has Failed to Satisfy a Prima Facie Case of Obviousness as the Cited Prior Art References Fail to Provide or Suggest All Claim Features of Claims 2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, And 24.

Claims 2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Apelgren and further in view of Yoon (U.S. Publication No. 2002/0090784). This rejection is traversed. Applicants submit that Apelgren, AAPA, and Yoon, individually or in combination does not disclose or suggest all of the features of claims 2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, and 24 as is required in a proper section 103 rejection.

To provide a prima facie case of obviousness against claims 2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, and 24, Apelgren, AAPA, and Yoon, individually or in combination must, at the very least, disclose or suggest the feature of scrubbing the low K dielectric layer having the plasma etched feature using a mixture fluid including a cleaning chemistry and a wetting agent where the wetting agent facilitates cleaning of the etch residues and the ashing residues with the cleaning chemistry. As established above in reference to section VII.A. above, Apelgren and AAPA individually or in combination do not disclose or suggest this feature as required to establish a case of prima facie obviousness as required in a section 103 rejection. As shown below the teachings of Yoon do not cure the deficiencies of the AAPA and Apelgren. Consequently, Applicants submit that combination of Apelgren, AAPA, and Yoon do not individually or in combination disclose or suggest all of the features of claims 2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, and 24.

The Yoon reference discusses wet etching methods for the removal of material (such as polysilicon films) and is therefore not applicable to the cleaning of residual

materials on hydrophobic surfaces after plasma etch and ashing processes. Yoon does not discuss or suggest the use of wetting agents or surfactants as applied to low-K dielectric (hydrophobic materials). The particular chemicals noted in Yoon (para. 48- NH_4OH, H_2O_2, and H_2O) etch polysilicon and oxide films but Applicants submit that they are not wetting agents such as surfactants that can render a hydrophobic substance cleanable by the cleaning chemistry.

To support the assertion that Yoon discloses usage of a surfactant with a cleaning solution, the Examiner makes the following statement on page 4 of the Final Rejection dated August 4, 2004,

"...Yoon discloses [wherein] the wetting agent is a surfactant and the cleaning chemistry includes a combination of NH_2OH, H_2O_2, and H_2O and deionized (DI) water."

To support the above assertion, the Examiner cites paragraph 48 of Yoon. Applicants respectfully direct the Board to paragraph 48 of Yoon which is provided below:

[0048] The first etchant has an etching rate in the ratio of about 1:1 to 1:1.5 with respect to polysilicon and oxide. Preferably, SC-1 (standard cleaning-1) solution including NH_4OH, H_2O_2, and H_2O, which are mixed in a ratio of 1:4:20, is used as the first etchant. The cleaning process using the first etchant is carried out for about 20 to 30 minutes in such a manner that polysilicon and oxide are etched in the range of 60 to 120 Å so as to completely remove the damaged layer 122 and the plate-shaped defect.

As can be seen, Yoon describes the use of NH_4OH, H_2O_2, and H_2O for wet etching applications, a concept unique from that of a surfactant or wetting agent for hydrophobic materials. As discussed above, Applicants submit that cleaning solution discussed above by Yoon is not a surfactant. Therefore Yoon makes no mention of the use of a wetting agent such as a surfactant with cleaning solution to clean etching and ashing residues from a low K dielectric. Therefore, Applicants respectfully submit that none of AAPA,

Apelgren, or Yoon discloses or suggests usage of a wetting agent such as a surfactant with cleaning solution to clean etching and ashing residues from a low K dielectric.

Accordingly, for at least the foregoing reasons, claims 2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, and 24 are patentable under 35 U.S.C. § 103(a) over Yoon, Apelgren or AAPA.

C. There Is No motivation to Combine AAPA with Apelgren to Suggest the Subject Matter of Claims 1, 8, 9, 10, and 17.

As will be explained below, there is no motivation to combine the teachings of Apelgren with AAPA to generate the claimed invention as defined by claims 1, 8, 9, 10, and 17.

Apelgren is directed to the removal of photoresist by chemical mechanical polishing and post polishing rinse. As known to those skilled in the art, one generally does not CMP low-K films or resist from low-K films in the integrated circuit fabrication process because low-K films are inherently subject to the damaging tensile stresses of the CMP process. Therefore, Applicants submit that one skilled in the art would not use the CMP process of Apelgren with low-k dielectrics as described in the present invention. Moreover, the rinsing of CMP residues from a photoresist removal process is materially different from the removal of residues following an etching of low-K materials and ashing process. The residues desired to be removed by the two processes are known by those skilled in the art to be different in chemical makeup and concentration. For example, the residues remaining after CMP removal of photoresist on silicon dioxide following an etch process generally include silicon dioxide, pad particulates, slurry, polymers and organics. Applicants submit that ashing residues are therefore not the same as the residues remaining after a CMP operation. In addition, Apelgren specifically denigrates ashing operations to remove photoresists from dielectrics by stating the problems of such operations. (See,

Apelgren, column 2, lines 5-15). Therefore, Applicants submit that one skilled in the art would not combine teachings related to the cleaning of etching and ashing residues (AAPA) with cleaning of post-CMP residues (Apelgren) especially when Apelgren discusses the drawbacks of using ashing to remove photoresist from dielectrics.

Moreover as discussed above in reference to Section VII.A, Applicants' background (AAPA pages 1-3) discloses that traditional methods of cleaning oxide films are inadequate for the cleaning of hydrophobic low-K dielectrics because typical oxides are hydrophilic and form different types of residues which require different types of cleaning methodology as compared to low K dielectrics (See, Specification, page 3, lines 13-17). Consequently, Applicants submit that one skilled in the art would not have been motivated to combine the disclosures of Apelgren and AAPA to generate a method for use of a wetting agent with a cleaning solution to clean etching and ashing residues on a hydrophobic material such as low-K dielectrics

D. There Is No Motivation to Combine AAPA, Apelgren, and Yoon to Suggest the Subject Matter of Claims 2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, and 24.

Applicants submit that there is no motivation to combine AAPA, Apelgren, and Yoon. As discussed above in reference to section VII.C. above, Applicants submit that there is no motivation to combine AAPA and Apelgren. Additionally, Applicants submit that one skilled in the art would not have combined Yoon with AAPA and Apelgren because Yoon discusses wet etching methods for the removal of material (such as polysilicon films) for solving a defect problem in semiconductor manufacturing and is therefore not applicable to the cleaning of residual materials on hydrophobic surfaces after plasma etch and ashing processes. As a result, Applicants submit that the Examiner is

attempting to combine the proverbial apples and oranges by mixing and matching disclosures from: 1) a reference that teaches wet etching of polysilicon and silicon dioxide for solving a defect problem (See, Yoon), 2) a reference that teaches cleaning of residues from a CMP operation (See, Apelgren) and denigrates usage of ashing operations, and 3) the AAPA which discusses the problems of cleaning ashing residues from a low-k dielectric surface. Therefore, Applicants submit that one skilled in the art would not have been motivated to combine Apelgren, Yoon, and the AAPA to generate the claimed invention.

E. AAPA, Apelgren, and Yoon Does Not Disclose or Suggest Usage of a Surfactant with Respect to Claims 2, 11, and 18.

As discussed above in reference to section VII.B, AAPA, Apelgren, and Yoon do not disclose or suggest cleaning etching and ashing residues from a low-k dielectric surface using a cleaning solution and a surfactant because none of Apelgren, AAPA, and Yoon even mentions usage of a surfactant.

F. The subject matter of claims 4, 5, 13, 14, 20, and 21 are not result effective variables in the context of MPEP § 2144.05.

Applicants respectfully submit that claims 4, 5, 13, 14, 20, and 21 are allowable for at least the reasons discussed in sections VII.B. and VII.D. The Examiner has stated that the concentrations of the solutions utilized is not inventive because it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. This rejection is traversed. Applicants

respectfully submit that routine experimentation with the solution disclosed in the Yoon reference would not have lead one having ordinary skill to the claimed cleaning solutions for several reasons. First, it is well established that a particular parameter must be recognized as a result-effective variable before the determination of the optimum or workable ranges of the variable might be characterized as routine experimentation. See M.P.E.P. § 2144.05. The Yoon reference does not provide one having ordinary skill in the art with any indication that a particular concentration of a surfactant is needed with a cleaning solution to effectively clean post etch and ashing residues from low-K dielectric materials. As a matter of fact, Yoon does not even mention a surfactant in its teachings. As such, because the Examiner has failed to establish that the art recognizes the allegedly optimized variables as being result-effective variables. Therefore, Applicants submit that the rejection of claims 4, 5, 13, 14, 20, and 21 are not proper under MPEP § 2144.05.

G. Conclusion

For the foregoing reasons, Applicants submit that the rejections under 35 U.S.C. §103 are in error and should be reversed.

Respectfully Submitted,
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APPENDIX A

CLAIMS ON APPEAL

1. (Previously Presented): A method for cleaning a semiconductor wafer, comprising:

plasma etching a feature into a low K dielectric layer having a photoresist mask, the plasma etching generating etch residues;

ashing the semiconductor wafer to remove the photoresist mask, the ashing generating ashing residues; and

removing the etching residues and the ashing residues from the low K dielectric layer having the plasma etched feature, the removing being enhanced by scrubbing the low K dielectric layer of the semiconductor wafer with a wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent.

2. (Original): A method for cleaning a semiconductor wafer as recited in claim 1, wherein the wetting agent is a surfactant and the cleaning chemistry includes a combination of NH_4OH, H_2O_2, and deionized (DI) water.

3. (Original): A method for cleaning a semiconductor wafer as recited in claim 2, wherein the surfactant is selected from a group comprising fluorosurfactants and hydrocarbon surfactants.

4. (Original): A method for cleaning a semiconductor wafer as recited in claim 3, wherein the surfactant has a concentration between about 0.005 percent by weight to about 0.1 percent by weight.

5. (Original): A method for cleaning a semiconductor wafer as recited in claim 3, wherein the surfactant has a concentration of about 0.01 percent by weight.

6. (Original): A method for cleaning a semiconductor wafer as recited in claim 2, wherein the combination ratio of NH_4OH, H_2O_2, and DI water is between about 1:4:10 and about 1:4:30.

7. (Original): A method for cleaning a semiconductor wafer as recited in claim 6, wherein the combination ratio of NH_4OH, H_2O_2, and DI water is about 1:4:20.

8. (Original): A method for cleaning a semiconductor wafer as recited in claim 1, further comprising:

scrubbing the low K dielectric layer using the brush while applying deionized (DI) water after removing the etching residues and the ashing residues.

9. (Previously Presented): A method for cleaning a semiconductor wafer, comprising:

plasma etching a feature into a low K dielectric layer, the plasma etching generating etch residues in and around the feature;

subjecting the semiconductor wafer to an ashing operation, the ashing operation generating ashing residues; and

scrubbing the low K dielectric layer having the plasma etched feature, using a mixture fluid including a cleaning chemistry and a wetting agent, the wetting agent being configured to condition the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry.

10. (Original): A method for cleaning a semiconductor wafer as recited in claim 9, further comprising:

scrubbing the low K dielectric layer using the brush while applying deionized (DI) water after removing the etching residues and the ashing residues.

11. (Original): A method for cleaning a semiconductor wafer as recited in claim 9, wherein the wetting agent is a surfactant and the cleaning chemistry includes a combination of NH_4OH , H_2O_2, and deionized (DI) water.

12. (Original): A method for cleaning a semiconductor wafer as recited in claim 11, wherein the surfactant is selected from a group comprising fluorinated surfactants and hydrocarbon surfactants.

13. (Original): A method for cleaning a semiconductor wafer as recited in claim 11, wherein the surfactant has a concentration between about 0.005 percent by weight to about 0.1 percent by weight.

14. (Original): A method for cleaning a semiconductor wafer as recited in claim 11, wherein the surfactant has a concentration of about 0.01 percent by weight.

15. (Original): A method for cleaning a semiconductor wafer as recited in claim 11, wherein the combination ratio of NH_4OH, H_2O_2, and DI water is between about 1:4:10 and about 1:4:30.

16. (Original): A method for cleaning a semiconductor wafer as recited in claim 11, wherein the combination ratio of NH_4OH , H_2O_2, and DI water is about 1:4:20.

17. (Previously presented): A method for cleaning a semiconductor wafer, comprising:

plasma etching a feature into a low K dielectric layer, the plasma etching generating etch residues in and around the feature;

subjecting the semiconductor wafer to an ashing operation, the ashing operation generating ashing residues;

scrubbing the low K dielectric layer having the plasma etched feature, using a mixture fluid including a cleaning chemistry and a wetting agent, the wetting agent being configured to condition the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry; and

scrubbing the low K dielectric layer having the plasma etched feature, using the brush while applying deionized (DI) water after removing the etching residues and the ashing residues.

18. (Original): A method for cleaning a semiconductor wafer as recited in claim 17, wherein the wetting agent is a surfactant and the cleaning chemistry includes a combination of NH_4OH, H_2O_2, and deionized (DI) water.

19. (Original): A method for cleaning a semiconductor wafer as recited in claim 17, wherein the surfactant is selected from a group comprising fluorinated surfactants and hydrocarbon surfactants.

20. (Original): A method for cleaning a semiconductor wafer as recited in claim 18, wherein the surfactant has a concentration between about 0.005 percent by weight to about 0.1 percent by weight.

21. (Original): A method for cleaning a semiconductor wafer as recited in claim 18, wherein the surfactant has a concentration of about 0.01 percent by weight.

22. (Original): A method for cleaning a semiconductor wafer as recited in claim 18, wherein the combination ratio of NH_4OH, H_2O_2, and DI water is between about 1:4:10 and about 1:4:30.

23. (Original): A method for cleaning a semiconductor wafer as recited in claim 18, wherein the combination ratio of NH_4OH, H_2O_2, and DI water is about 1:4:20.

24. (Previously Presented): A method for cleaning a semiconductor wafer, comprising:

plasma etching a feature into a low K dielectric layer, the plasma etching generating etch residues in and around the feature;

subjecting the semiconductor wafer to an ashing operation, the ashing operation generating ashing residues;

scrubbing the low K dielectric layer having the plasma etched feature, using a mixture fluid including a cleaning chemistry and a wetting agent, the wetting agent being configured to condition the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry, the wetting agent being a surfactant and the cleaning chemistry being a standard clean-1 (SC-1) solution including a combination of NH_4OH , H_2O_2, and deionized (DI) water, the surfactant having a

concentration between about 0.005 percent by weight to about 0.1 percent by weight, combination ratio of NH_4OH , H_2O_2, and DI water being between about 1:4:10 and about 1:4:30; and

scrubbing the low K dielectric layer having the plasma etched feature, using the brush while applying deionized (DI) water after removing the etching residues and the ashing residues.